A NONLINEAR GaAs FET MODEL FOR USE IN THE DESIGN OF OUTPUT CIRCUITS FOR POWER AMPLIFIERS

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Abstract

A nonlinear equivalent circuit model for the GaAs FET has been developed based upon the small-signal device model and separate current measurements, including drain-gate avalanche current data. The harmonic balance technique is used to develop the FET rf load-pull characteristics in an amplifier configuration under large signal operation. Computed and experimental load-pull results show good agreement.

Introduction

Tajima and Miller [1], Willing et al. [2], Peterson et al. [3] and others have reported nonlinear GaAs FET models for the design of power amplifiers. We have extended the work of Peterson et al. and made detailed comparison of computed and measured load-pull characteristics using a nonlinear analysis program for the GaAs FET amplifier based upon the harmonic balance technique [4].

Our nonlinear device model has evolved from the self-consistent GaAs FET small-signal model reported by Curtice and Camisa [5]. The program provides a computer-aided means to develop output circuit designs that optimize the amplifier performance (i.e. efficiency, bandwidth, etc.). Accurate prediction of large-signal load pull performance is essential to accuratly design output networks. In addition, we operate the program on Hewlett-Packard 1000 RTE minicomputers to reduce the cost of computation.

The Nonlinear FET Program

The program consists of a time-domain model of the GaAs MESFET coupled with frequency domain models for the input and output matching circuits. The nonlinear FET elements must be analyzed in the time domain to preserve their physical nature. The linear circuit response to the FET current excitation can be analyzed in the frequency domain by standard techniques. Transformation between time and frequency domains is accomplished using a fast Fourier transform. A valid physical solution is obtained when the voltage waveform at the input (or output) of the FET produces a current waveform into the device that is the negative of that into the rf circuit within some small error. The program flow chart is shown in Fig. 1.

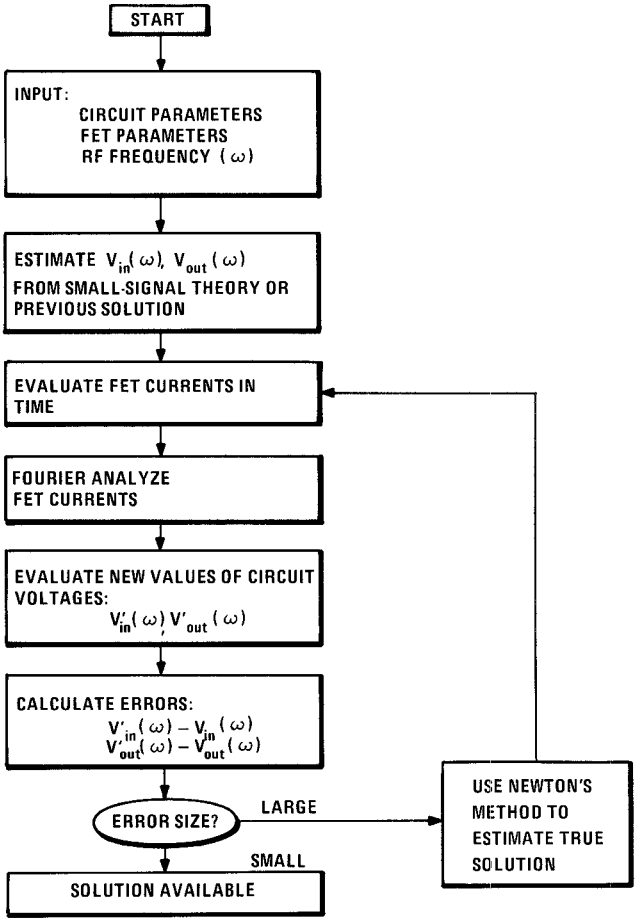

Fig. 1. Program flow chart.

Evaluation GaAs MESFET Nonlinearities

Figure 2 shows the equivalent circuit model assumed. This model is noticeably different than used by Curtice and Camisa for accurate small-signal modeling of GaAs MESFET's. The drain-channel capacitor is omitted to simplify node current equations. This produces some loss of accuracy. In addition, two new current sources are used. The drain-gate voltage-controlled current source represents the drain-gate avalanche current that can occur at large-signal operation. The gate-source

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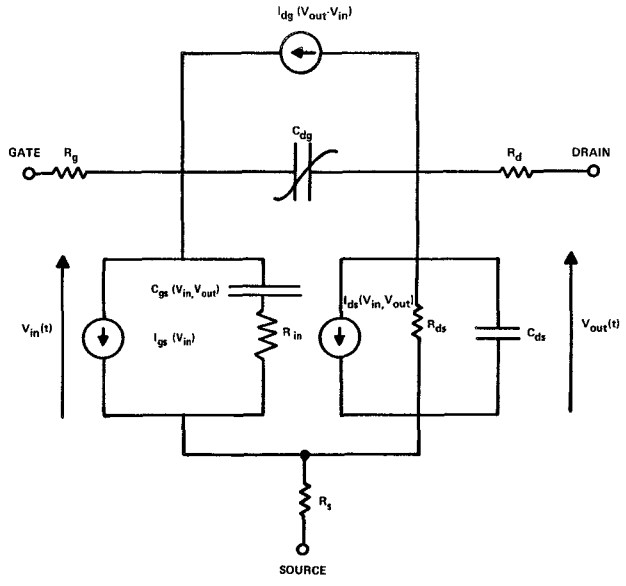

Fig. 2. Equivalent circuit model of the GaAs MESFET.

voltage controlled current source represents gate current that occurrs when the gate-source junction is forward biased. The third current source, $I_{ds}(V_{in},V_{out})$, is the large signal form of the usual small-signal transconductance.

The dc current-voltage relationship data is measured in the automated Fukui [5] equipment and Kelvin probes are used (and required) to obtain accurate data. The device pinch-off voltage increases appreciably at larger drain-source voltage. The early version of the nonlinear program assumed a square-law relationship between the (saturation) current and the gate-source voltage. Although this form has advantages, it is more accurate to use a cubic approximation:

$$I_{ds} = (A_0 + A_1V_1 + A_2 V_1^2 + A_3 V_1^3)\cdot\tanh(\gamma\cdot V_{out}(t))$$

where V_1 is the input voltage. The coefficients (A_i) can be evaluated from data in the saturation region at the same time the current-voltage data is measured. We use a simple FORTRAN program for evaluation of the A_i's with least square error. One disadvantage of the cubic relationship is that unlike the quadradic, a pinch-off voltage may result that makes current zero or transconductance zero, but not both.

The following method is used to include the phenomenon of pinch-off voltage increase with drain-source voltage. We assume:

$$V_1 = V_{in}\ (t\text{-}\tau) \cdot [1 + \beta\ (V^o_{out} - V_{out}(t)]$$

where β = coefficient for pinch-off change

V^o_{out} = output voltage at which A_o, A_1, A_2, A_3 were evaluated

and τ = internal time delay of FET. The form of this equation is not physically significant.

Measured rf data shows that τ is a direct function of drain-source voltage, or

$$\tau = A_5 \cdot V_{out}(t)$$

Pulsed measurement of drain-gate avalanche currents are made using 20 nanosecond pulse width. The drain currents cannot be pinched off at large drain-source voltages due to the gate current produced by avalanche breakdown. This is an important phenomenon that limits both rf current and power output.

The values of R_g, R_d and R_s are obtained from the automated Fukui measurements. The values of C_{dg}, C_{gs}, R_{ds} and C_{ds} at the bias point are obtained from the small signal model using the technique developed by Curtice and Camisa. Although both C_{gs} and C_{dg} are nonlinear functions of voltage, computation including these characteristics produced only small effects upon the rf saturation characteristics.

Description of the Computer Program NFET

Figure 3 shows the lumped-element equivalent circuit model of the GaAs MESFET amplifiers. The two-port networks $[Y_{in}]$ and $[Y_{out}]$ are matching networks presumably designed for maximum power transfer at the input and the output, respectively. Notice that the gate and drain resistances of the FET are absorbed into these networks. The first design of these networks is usually done using SUPER-COMPACT [6] to achieve conjugate matching at input and output for small-signal operation. This produces the maximum gain condition. Once a trial design is available, the Y-transfer characteristics can be evaluated.

The time domain expressions for $V_{in}(t)$ and $V_{out}(t)$ are used to generate device currents. For example, the total drain current consists of drain source current:

$$I_{ds}[V_{in}(t),V_{out}(t)] + C_{ds}\frac{d}{dt}V_{out}(t) + \frac{V_{out}(t)\text{-}V^{dc}_{out}}{R_{ds}}$$

plus drain gate displacement current:

$$C_{dg}\ \frac{d}{dt}\ [V_{out}(t) - V_{in}(t)]\ ,$$

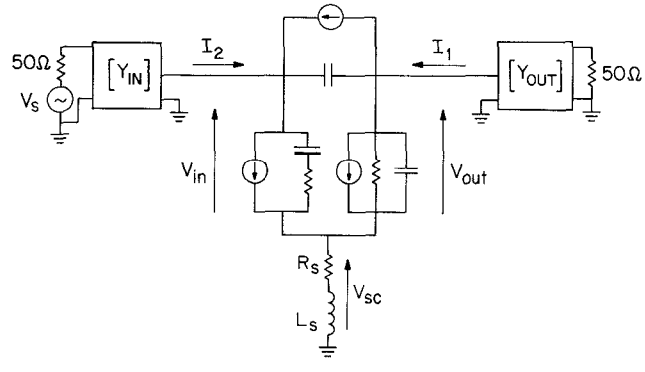

Fig. 3. Equivalent circuit model of GaAs MESFET amplifier as used in the nonlinear analysis program.

and the avalanche current if $[V_{out}(t) - V_{in}(t)] >$ the breakdown voltage, V_B.

The drain and gate currents are then Fourier analyzed to find their frequency components using a fast Fourier transform. Linear circuit elements, such as C_{dg} need not be included since the answers are known a priori.

Comparison with Experimental Data

Fundamental and second harmonic voltages are used for the calculation presented in this section. Figure 4 shows the calculated rf power output as a function of rf power input for RCA device B1512-3A for two cases of output matching. Strong output power saturation occurs due to the large rf voltage amplitudes for the case of high small-signal gain (167 Ω). By reducing the shunt resistive loading of the output circuit, higher rf power output can

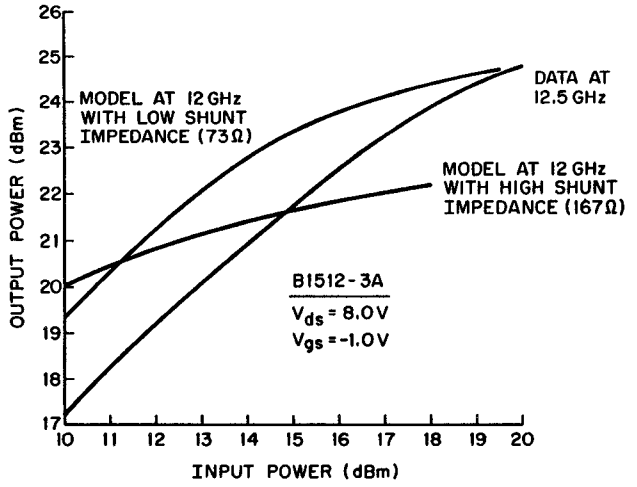

Fig. 4. Measured and calculated rf power output as a function of rf power input for device B1512-3A with V_{ds} = 8 V, V_{gs} = - 1 V and plotted as a logarithmic scale.

be achieved. The case of lower shunt impedance (73 ohms) is very similar to the measured data. There is about 2 dB difference in the power gain for the data and the lower shunt impedance case. A portion of the 2 dB is believed to be due to input tuner losses in the tuner used in the measurements.

Figure 5 shows the effect of harmonic voltages upon the input/output power calculated for this device with optimized output loading. Note that neglecting the second harmonic significantly changes the output power in the saturation region. However, it is difficult to evaluate accurately the impedance seen at each harmonic in a given circuit. The impedance used for this calculation assumes lumped element matching.

Figure 6 shows the calculated load pull contour for 175 mW output power for a second RCA device at 50 mW rf input power. In the experiment, the rf input power was 104 mW. Figure 7 shows the same comparison for an output power of 150 mW with the same drive conditions. There is good agreement with regard to output load pull characteristics for a given output power, but disagreement in driver power (and gain) by approximately 3 dB. Some of

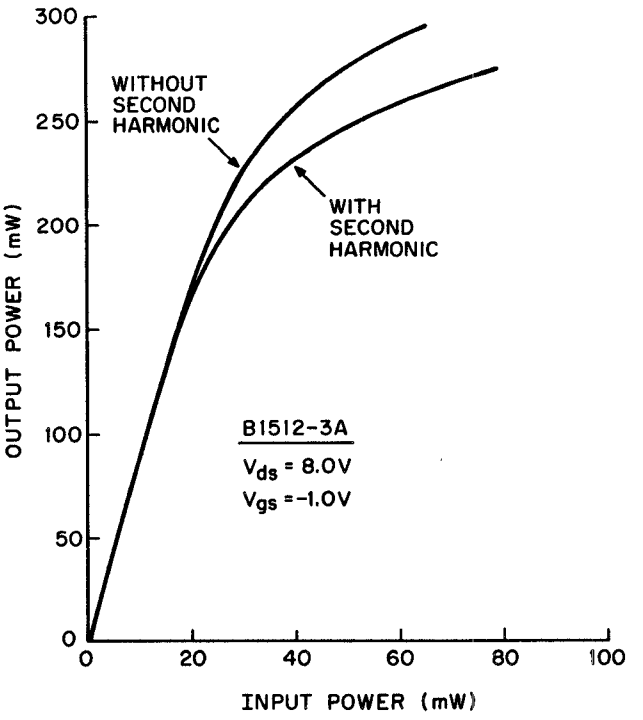

Fig. 5. RF output versus input calculated with and without second harmonic voltages for device B1512-3A at 12 GHz.

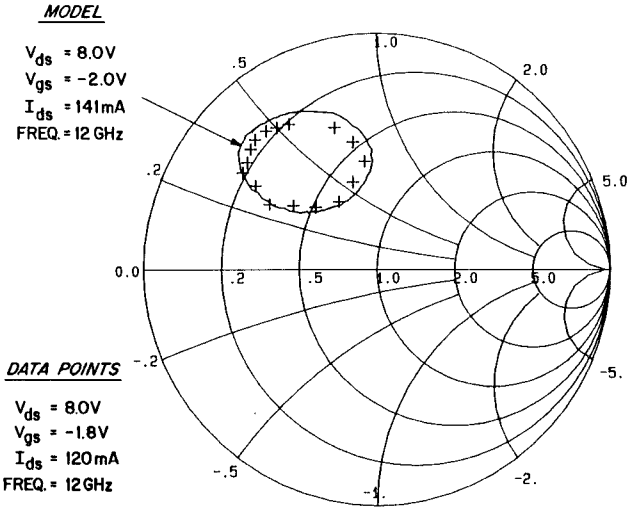

Fig. 6. Smith chart display of calculated and measured rf output loads for constant output power of 175 mW for device B1824-1C at 12 GHz.

this error is attributable to losses in the input tuner used in the measurements.

The maximum rf power output for the simulation with 50 mW input power is 216 mW. In the experiment using 104 mW rf drive, the maximum rf power output was 205 mW.

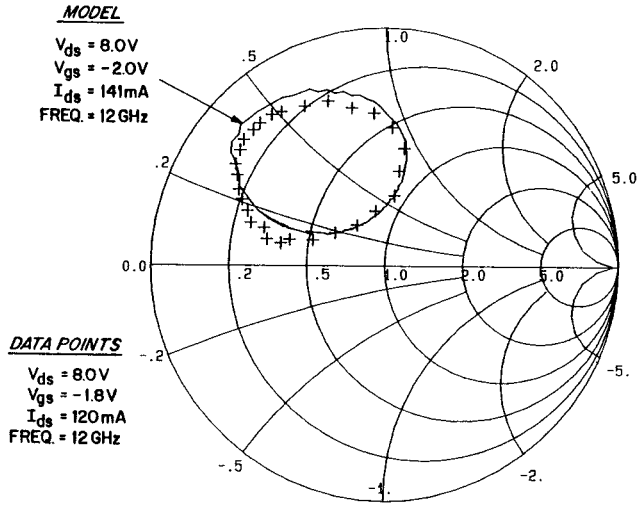

Fig. 7. Smith chart display of calculated and measured rf output loads for constant output power of 150 mW for device B1824-1C at 12 GHz.

Figure 8 shows the load conditions for maximum power output at seven different output power values as computed by the nonlinear program. Measured data are also shown and are in good agreement.

A comparison was made with large-signal simulations using an accurate two-dimensional model for the GaAs FET. This model includes carrier heating effects that produce the phenomenon of velocity overshoot. The output current and voltage waveforms in time could be directly compared for this case and the harmonic power contents were found to be in good agreement.

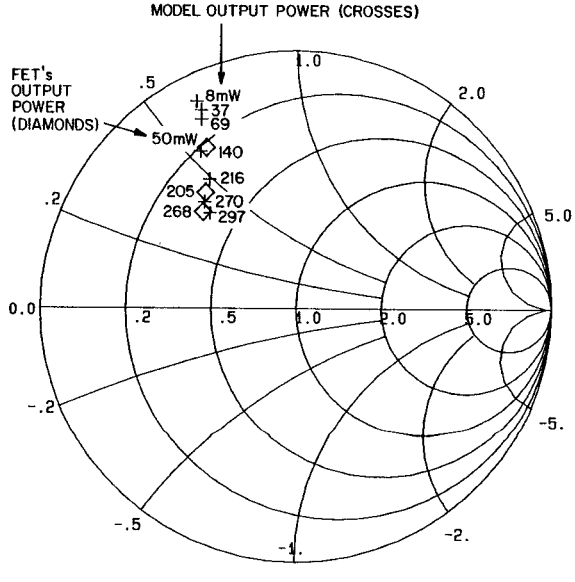

Fig. 8. Smith chart display of calculated and measured optimum rf output loads for device B1824-1C at 12 GHz.

Conclusion

We have developed an FET model suitable for efficient calculation in the large-signal region. It is useful for developing optimized output network designs for high power GaAs FET amplifiers. The program efficiency results from the use of the harmonic balance technique wherein the nonlinear FET is analyzed in the time domain and the linear circuit is analyzed in the frequency domain.

The principle nonlinearities of the FET are voltage-controlled current sources. The nonlinearity of the reactive elements does not affect the large signal solution greatly. However it is necessary to evaluate the characteristics of the current sources for each device to be simulated. The simulation can be performed with voltage waveform containing fundamental and second harmonic frequencies or fundamental, second harmonic and third harmonic frequencies. All FET current harmonics are included. Third harmonic is only used when accurate circuit impedance data is available at third harmonic frequency.

The nonlinear FET model was coupled to a program to generate constant output power contours on a Smith chart. Excellent agreement was obtained with the measured load pull characteristics at 12 GHz. However, the simulation predicted more gain than was measured in the experiments.

Acknowledgment

The authors are indebted to Dr. B. S. Perlman of RCA Laboratories for guidance in the program and for many helpful discussions, to S. M. Perlow (RCA) for making the load-pull measurements to D. L. Rhodes (RCA) for the graphics software and to P. D. Gardner (RCA) for device measurements.

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